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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,564	09/10/1999	HOWARD THOMAS OLNOWICH	EN997080B	4402

7590 10/27/2003

IBM Corporation
Intellectual Property Law (Dept. 917, Bldg. 006-1
3605 Highway 52 North
Rochester, MN 55901-7829

EXAMINER

BATAILLE, PIERRE MICHE

ART UNIT	PAPER NUMBER
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2186

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DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/394,564

Applicant(s)

OLNOWICH, HOWARD THOMAS

Examiner

Pierre-Michel Bataille

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) 2 and 30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 31-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is taken in response to Applicant communication/request for reconsideration filed August 25, 2003 in response to Non-Final Action dated July 17, 2003. Claim 2-30 have been canceled; Claims 1 and 31-39 are pending in the application under examination. Applicant's amendment and/or arguments have been considered with the results that follow.

Response to Arguments

2. Applicant's arguments filed August 25, 2003 have been fully considered but they are not deemed to be persuasive for at least the following remarks.

Applicant admits that the applied reference, US 6,249,520 (Steely, Jr. et al) correctly teaches multiple aspects of the invention, such as shared memory parallel processing system having a cache coherency system including a plurality of nodes interconnected through an interconnecting network. Applicant further admits that both the claimed invention and the applied reference use a shared memory system as backdrop for teaching the respective invention, but argues that the prima facie case of anticipation is not made in the examination of the present application. Applicant, specifically, argues that the cache coherency system claimed in the present application differs from the applied prior art reference, referencing that the applied prior art reference fails to teach "an adapter for storing changed data immediately to said unique section of shared memory regardless of which said node is changing the data and

which of said nodes includes the section of shared memory to be changed, wherein said shared memory always contains the most recent data".

Although the applied reference by Steely, Jr. has some distinctive features from the descriptive features of the present invention, the distinction is not featured in the claims in such a way that makes the distinction non-expressive. In other words, applicant's arguments do not remove the reference from reading on the claims. The claims requires "an adapter for storing changed data immediately to said unique section of shared memory regardless of which said node is changing the data and which of said nodes includes the section of shared memory to be changed, wherein said shared memory always contains the most recent data". Steely, Jr. provides the equivalent of the argued feature. Steely Jr. explicitly describes store operations by control logic considered complete as soon as invalidate messages have been posted to the other nodes, making the most updated data available [Col 14, Lines 42-50]. The changing node does not care or made sure the invalidation signal is received or whether the other nodes receiving the invalidation message invalidate their respective cache.

Applicant, on page 37-38, explains that Steely, Jr. describes a cache coherent protocol which is an ownership protocol because there is always an identifiable 'owner' of each memory line and further argues that the process of Steely, jr. includes all sorts of complexities such as invalidates, clean to dirty transactions. In contrast to the alleged simplicity of the claimed invention, which does not requires such complexities, the claims, similar to the applied prior art, require "a cache coherency directory is distributed

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to each of said nodes for tracking which of said nodes have copies of each cache line", which explicitly features ownership information, as in Steely, Jr.

In view of the above, anticipation is proven, the applied reference is nor withdrawn and the applied rejection is maintained and repeated below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 31-39 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,249,520 (Steely, Jr. et al).

With respect to claims 1 and 31-34, Steely, jr. discloses, as required in the claims, a cache coherency system and method for operating a shared memory parallel processing system including a plurality of processing nodes [(a large symmetric multi-processor including a plurality of the multi-processing nodes) Fig. 7; Col. 12, Lines 56-63; Col. 13, Lines 16-22] comprising:

a multi-stage communication network for interconnecting said processing nodes [(a large symmetric multi-processor may be provided by interconnecting a plurality of

the multi-processing nodes via a hierarchical switch 155) Fig. 7; Col. 12, Lines 56-63;
Col. 13, Lines 16-22];

each processing node including a unique section of shared memory which is not a cache [(large SMP system is a distributed shared memory system, wherein each of the multi-processing nodes 100a-100h includes an addressable portion of either the overall system memory or a sub-divided portion of physical memory) Col. 13, Lines 32-37; Col. 14, Lines 12-19];

each processing node including one or more caches for storing a plurality of cache lines [each of the multi-processor nodes including elements for maintaining memory coherency, including a cache memory (14c Fig. 2 & 6) and a victim cache (124, Fig. 6), a directory); Abstract; Col. 16, Lines 57-63; Col. 16, Lines 19-39];

a cache coherency directory is distributed to each of said node for tracking which of said nodes have a copy of each cache line [each of the multi-processor nodes including elements for maintaining memory coherency including a directory (IOP tag 14b Fig. 2&6 and DTAG 20, Fig. 2 & 6)); Abstract; Col. 16, Lines 63-67; Col. 16, Lines 43-56]; and

an adapter for storing changed data immediately to said unique section of shared memory regardless of which of said node is changing the data and which of said nodes includes the section of shared memory to be changed, such that said shared memory always contains the most recent data [(store operations by control logic are considered complete as soon as invalidate messages have been posted to the other nodes, making the most updated data available) Col 14, Lines 42-50].

With respect to claim 35, Steely, Jr. discloses the shared memory including a first memory portion for storing unchangeable data and a second memory portion for storing changeable data [Col. 14, Lines 22-30; Col. 18, Lines 18-64] and said cache coherency directory listing which node of said plurality of processing nodes have accessed copies of said cache line in said second memory portion [Col. 16, Lines 43-67; Col. 18, Lines 18-64].

With respect to claim 36, Steely, Jr. discloses each of said plurality of processing nodes being operable for reading, storing, and invalidating said shared memory at any other of said processing nodes [Col. 16, Lines 19-33; Col. 18, Lines 18-64].

With respect to claims 37, Steely, Jr. discloses each processing node having a memory controller operable to respond to requests for access a memory word in cache at a first node [Col. 17, Lines 20-36; Col. 18, Lines 18-64] and if not available in cache, accessing said memory word from the shared memory regardless of which processing node includes the section of shared memory being accessed and storing said cache line in the cache at said first processing node [Col. 17, Lines 20-36; Col. 18, Lines 18-64].

With respect to claims 38-39, Steely, Jr. discloses the controller being operating to delete a cache line to provide space for a new cache line and sending an invalidation directory to indicate said node no longer has a copy of the cache line [Col. 16, Line 61 to Col. 17, Line 5; Col. 18, Lines 18-64], and said controller operative to send cache update message to update corresponding cache line having copy of changed cache line and for receiving cache lines of data from remote nodes [Col. 18, Lines 18-64].

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,049,889 (Steely, Jr. et al) teaching high performance recoverable communication method and apparatus for write-only networks.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

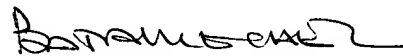
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone

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numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



Pierre-Michel Bataille
Primary Examiner
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October 18, 2003